Remarks

Claims 1-31 are pending in the application. All claims stand rejected. By this paper, claims 1, 9, 17, 20, 24, and 28 have been amended. Reconsideration of all pending claims herein is respectfully requested.

Claims 1-31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Stracovsky et al. ("Stracovsky") in view of Katayama et al. ("Katayma"). As amended, claim 1 recites:

> detecting a write data burst;
>
> determining if at least one memory unit is available to receive the write data burst;
>
> writing the write data burst to the at least one memory unit if the at least one memory unit is available to receive data;
>
> storing a first portion of the write data burst in a buffer, concurrently with activating the at least one memory unit to receive data, if the at least one memory unit is not available to receive data;
>
> writing a second portion of the write data burst to the at least one memory unit when the at least one memory unit is available to receive data without storing the second portion in the buffer; and
>
> writing the first portion of the write data burst from the buffer to the at least one memory unit after writing the second portion of the write data burst.

Similar amendments have been made to independent claims 9, 17, 20, 24, and 28.

In reference to claim 1, the Examiner states that Katayama teaches "writing a first portion of write data burst in a buffer (52, figure 2) concurrently with activating at least one memory unit if the at least one memory unit is busy." This limitation is found in the independent claims 1, 9, 17, 20, 24, and 28, but these claims also require that the memory unit must be busy as a condition for a first portion to be written to a buffer.

In Katayama, all data units are temporarily retained in the write buffer 52 whether or not the DRAM array 22 is busy. Col. 18, lines 9-13. All data units are then written from the write buffer 52 to the bit switch 26. Col. 21, lines 51-52. Thus, Katayama does not require that the DRAM array 22 must be busy as a condition for storing data units in the write buffer.

Katayama teaches that the DRAM array 22 is never busy for a write and read operation. Instead, read, write, and refresh operations are timed so as not to interfere with one another. See Figures 3-5 and accompanying text. Figure 2 illustrates on the right-hand side the different operations (AL, ET, RD, CD, AR, PR, TR) that occur in the generally indicated locations in the circuit. As shown in Figures 3-5, the AR (array access) and PR (precharging) operations in the DRAM array 22 are timed so as not to occur at the same time. Thus, the DRAM array 22 is never accessed or charged at the same time.

When a refresh operation is required, Katayama times the refresh operation so as not to interfere with an array access. In the case of write operations, Katayama times the refresh operations to initiate during a cycle during which the third unit data of the write data comprising four unit data is transferred. Col. 22, lines 36-32. By timing operations, data transfer is constant, bus efficiency is 100 percent, and data can be written to the DRAM array 22 in a constant and short access time whether or not refreshing is being executed. Col. 22, lines 37-44.

Claim 1 recites storing a data portion in a temporary buffer if an intended memory unit is busy. If the memory unit is not busy, then the data portion is not stored in the temporary buffer as there is no need. By contrast, Katayama teaches

that the DRAM array 22 is not to be busy during a data transfer and all data units pass through the write buffer 52.

Claim 1, as well as independent claims 9, 17, 20, 24, and 28, have been amended to include the limitation that the second portion is written to the memory unit when the memory unit is available and without storing the second portion in the buffer. The present Application describes storing the second portion directly in a memory unit to increase efficiency. Temporarily storing the second portion in a temporary buffer defeats this purpose. By contrast, Katayama teaches that all data units are temporarily stored in the write buffer 52. This is in keeping with the purpose of Katayama which relies on parallel timing of operations to improve bus efficiency, whereas the present Application describes partial storage of data bursts in a temporary buffer to improve bus efficiency. Thus, Katayama does not disclose or suggest partial storage of a data burst in a temporary buffer.

Neither Stracovsky or Katayama independently or in combination teach or suggest the temporary storage of one portion of data burst in a buffer while passing another portion directly to a memory unit. This feature is completely absent in the cited references. Neither Stracovsky or Katayama independently or in combination teach or suggest storing a first portion of a data burst in a buffer with the condition of a memory unit being busy.

"To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." MPEP § 2143.03. None of the cited references, alone or in combination, disclose the limitations discussed above. Hence, claims 1, 9, 17, 20, 24 and 28 are believed to be patentably distinct.

All other claims depend directly or indirectly on one of these claims and are likewise believed to be patentably distinct for at least the same reasons. In view of the foregoing, reconsideration and early allowance of all pending claims herein is respectfully requested.

Respectfully submitted,

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